REMARKS

The preamble of claim 116 has been amended in response to the rejection of claims 116-127 under 35 U.S.C. 112, second paragraph. Since claims 101-115 are being cancelled, this is the only section 112 rejection to which a response is necessary.

The rejections of the remaining claims in this application over various combinations of prior art under 35 U.S.C. 103 are discussed below. The following cited prior art is discussed below: Australian patent no. 22536/83 ("Burke"), European patent application publication no. 0 220 718 ("Yorimoto *et al.*"), and U.S. patents nos. 4,774,700 ("Satoh *et al.*") and 4,525,839 ("Nozawa *et al.*"). For the reasons stated below, it is respectfully submitted that the cited references would not have rendered the claims of the present application obvious to one ordinarily skilled in the art before April 13, 1989, the effective filing date of the present application.

Summary of Argument

The claims are directed to a flash EEPROM system, or to the use and operation of such a memory system, that includes its own controller. The memory controller both makes it possible for the host system to communicate with the memory system and controls operation of the flash EEPROM cell array. The memory cell array is divided into sectors, with the cells within each sector being erasable together as a unit. Stored in each sector is a sectors worth of user data and some overhead information (a header) about the sector and/or about the user data stored in the sector.

The claimed memory system looks to the host computer as if it was a disk drive system, similar to the goal stated in the cited Burke patent. But a significant difference is the claimed operation of the flash EEPROM array with many incidents of a disk system. It is divided into sectors that are operated as a unit, including overhead data (a header) as well as user data, and, in some of the claims, the overhead data is read from an addressed sector before user data is written into that sector.

This is quite different from the way that semiconductor memory arrays are usually operated. Data is usually written to or

read from a RAM by first addressing one storage location, holding one or a few bytes of data, and then incrementing through adjacent storage locations in sequence until an entire data file is written or read. The present claims, however, define a disk like approach to semiconductor memory operation. The fact that the system of the Burke patent may look to the host system as a disk memory system does not mean that its array is operated in sectors, with headers, etc., as claimed. While sector addressing may be used between a host and the controller, the host does not know or care what type of addressing is being used between the controller and the memory media. In the case of a magnetic disk media, its physical attributes have naturally resulted in sector addressing by the controller. But for a random accessed solid state memory, it is more efficient to address the memory by large files, such as one that is transferred by a DMA (Direct Memory Access) controller. As a general proposition, a memory system controller can manipulate and rearrange storage of data in the semiconductor memory in any number of ways while the controller makes the memory system appear to the host system as a disk drive memory.

Furthermore, with regard to the storage of a header (overhead data) along with user data of individual sectors, it includes auxiliary information being used by the controller to properly and efficiently access particular sectors, given the particular physical characteristics of the memory medium. It is in the nature of semiconductor RAMs, however, that no such auxiliary information is required to access the memory itself.

However, the flash EEPROM system employed in the present invention, unlike typical RAMs, do have memory operations that can benefit from auxiliary information. The provision for making such information available in a header of each sector in the context of a solid state memory is part of the present invention.

An underlying assumption made throughout the Examiner's Action is that it is *inherent* in the system of the cited Burke reference to operate its volatile RAM array with sectors, and thus obvious to include overhead data (headers) in individual sectors. This premise, and thus all the rejections based upon it, is respectfully submitted to be incorrect. Contrary to the position

taken in the Examiner's Action, it is submitted that the fact that Burke's system looks to the host system as a disk drive memory does not compel this conclusion. The alleged inherent Burke disclosure upon which nearly all the grounds of rejection are based does not exist.

Application of the doctrine of "inherency" is not appropriate in this case. As noted by the court in Ethyl Molded Products Company v. Betts Package Inc., 9 U.S.P.Q. 2d 1001, 1032-1033 (E.D. Kentucky, 1988):

> The doctrine of inherency is available only when the prior inherent event can be established as a certainty. That an event may result from a given set of circumstances is not sufficient to establish anticipation. Probabilities are not sufficient . . . A prior inherent event cannot be established based upon speculation, or where a doubt exists.

In this case, the operation of the semiconductor memory of Burke that is found to be "inherent" is not at all certain but rather is a conclusion formed simply from the fact that the memory interfaces to the host system with a sector format. There can be no doubt that this determination lacks the required certainty. It is thus respectfully submitted that all the outstanding rejections based thereon must be withdrawn.

It is also respectfully submitted that the Official Notice of prior art "facts" taken extensively throughout the Examiner's Action is in error. This procedure is proper for facts that are unquestionably well known in the art or generally known but is not proper to establish technical facts that are not well known or which are in esoteric technology. See the M.P.E.P., section 2144.03, Sept. 1995. As discussed below with respect to specific facts attempted to be established in the Examiner's Action by taking Official Notice of them, those facts are far from being generally known. They pertain to quite detailed aspects of computer memory technology. The taking of Official Notice of such facts in submitted to be improper.

Furthermore, it is respectfully submitted that certain of the alleged "facts" are not correct. An example is the assertion that ".. it is known in the art that the information bits in a

group of bit-storing units (called sector) in a magnetic memory device are erasable together as a unit;" (Examiner's Action, p. 10, para. d). But the fact is that sectors of magnetic memories are not individually erased during operation. They are simply written over with new data when required. If there is some existing prior art that describes a magnetic disk system where the sectors are individually erasable as a unit, it should be cited since this is certainly not the common practice. It is definitely not appropriate to take Official Notice of such a fact for the purpose of rejecting claims.

Claims 79-84, 98 and 99

Reconsideration is respectfully requested of the rejection of independent claim 79, and its dependent claims 80-84, 98 and 99, as obvious over a combination of the cited Burke, Yorimoto *et al.* and Satoh *et al.* references, as well as certain facts of which Official Notice is being taken. In rejecting claim 79, the Examiner's Action states the following: "Burke's memory system includes an array of cells which are inherently partitioned into a plurality of sectors because Burke's array is to 'emulate' a magnetic disk which has sectors." (Examiner's Action, p. 4.) This is the assumption about Burke which, as discussed in the preceding section, is believed to be in error. Yorimoto *et al.* is then cited as evidence that it would have been obvious to partition Burke's inherent sectors into user data and overhead data portions. Satoh *et al.* is further cited as evidence that it would have been obvious to provide for substitution of a useable sector for an unusable sector of the Yorimoto *et al.* modified Burke inherently sectored memory.

It is respectfully submitted that the basis expressed for the rejection is in error. The claims in this application each define more than the desire to make a semiconductor memory system look on the host system side of the memory controller to be a disk drive. They define a way of configuring and using a semiconductor memory on the memory side of the controller in a way similar to a disk drive. Claim 79 defines a flash EEPROM system with an array that is divided into sectors of cells that are erasable together as a unit. This is not new by itself but is a particular type of

memory which is recited by claims 79-84 to be used to emulate a disk drive. None of the three cited references suggest use of such a type of memory. The only mention of an EEPROM system is by Yorimoto *et al.* but their embodiments appear to be generically described for use with either an EEPROM or a battery backed volatile RAM. Nothing is said by Yorimoto *et al.* of a flash EEPROM system that is operated with sectors of cells that are erasable together as a unit. It is the use of this type of memory that allows the memory itself to be operated very similarly to that of a disk drive, with individual sectors that store both user data and overhead data (a header for the sector). It is the operation of the flash EEPROM memory by the memory controller with the sectored and partitioned characteristics of a disk drive memory that is novel and non-obvious.

The disclosure by Burke of his semiconductor memory system "emulating a rotating magnetic memory device" certainly does not suggest that his controller operates the semiconductor memory in the claimed sectored and partitioned manner. There is nothing "inherent" from the expressed disk emulation that suggests that Burke operates its semiconductor memory in the sectored manner being claimed. What the emulation states is that the controller interfaces with the host computer system as if it is a disk drive but the controller could operate the semiconductor memory in any number of ways. Although Burke discloses operating his semiconductor memory in groups of 64K cells, it appears that his controller interfaces with and operates the semiconductor memory in traditional ways, rather than emulating disk drive memory sectors. One skilled in the art, it is submitted, would therefore not have found it obvious to apply the sector partitioning technique of Yorimoto *et al.* It is not seen how one skilled in the art could have found it obvious to form a combination of such different memory architectures.

It is further not understood what type of block substitution in the Burke system would the disk drive system of Satoh *et al.* have suggested to one ordinarily skilled in the art. Would it be substitution of one of Burke's large 64k groups for another? It is submitted that it would not have been obvious to

apply the disk drive substitution technique of Satoh *et al.* to Burke's memory. But also important is that none of the three references cited against claims 79-84 suggest a sectored flash EEPROM system where the cells of the individual sectors are erasable together, let alone the use of the disk drive techniques of a header (overhead data) and unusable sector substitution to such a defined flash EEPROM sector.

Dependent claims 80 and 81 recite that a sector is replaced because a certain number of cells of the sector are defective. It is believed to be quite unusual, if it has ever occurred in the prior art, for defects in volatile semiconductor RAMs (as in the Burke reference) to be handled by throwing away such a large proportion of a memory, much of which would likely remain good. The rejection of claim 81 is predicated upon Official Notice being taken of certain facts (Examiner's Action, p. 6, first paragraph). It cannot be accepted that the prior art fact there alleged to exist is "notoriously old and well known" but it can be pointed out that defect management prior art has been made of record in this application. It is requested that any further rejection of claim 81 be based upon actual prior art rather than that believed by the Examiner to exist.

With respect to claim 82, the Examiner's Action states that "The size of 512-bytes, which is took (sic.) as a given amount of user data, is of obvious design choice." But the point of this claim is that the flash EEPROM memory is sectored exactly like the disk drive which it emulates. The memory controller does more than just appear to the host computer system to be a disk drive, it operates the flash EEPROM cell array like a disk drive. New claim 144, also dependent upon claim 79, recites that the disk drive and flash EEPROM formats are the same in that each carries substantially the same amount of data.

Claim 83 adds to the combination of claim 79 that the overhead data (header) in the individual flash EEPROM sectors includes the address of the sector in which it resides. This further defines the unique operation of the flash EEPROM system to operate as a disk drive. Claim 84 recites that the overhead data

of a sector includes an error correction code (ECC) that has been calculated from the user data stored in the same sector.

Dependent claims 98 and 99 have been rejected as obvious over the same three references as their parent claim 79, plus some alleged prior art about which Official Notice has been taken. These dependent claims add to the method of claim 79 two techniques for linking the address of a usable sector with an unusable one, in the course of sector substitution. It cannot be accepted that alleged facts a. through f. on page 6 the Examiner's Action ".. are notoriously old and well known in the art of memory patching." Nor can it be accepted that one ordinarily skilled in the art would have been motivated to use this alleged notoriously old prior art in the was suggested in subparagraphs a-d on page 7 of the Examiner's Action. Certain prior art of defect management of flash EEPROM systems has been made of record, and it is suggested that any further rejection of these claims be based upon actual prior art. To the extent that the Examiner's Action is taking Official Notice of some of the facts a.-f. allegedly being true with regard to disk drive memory systems, it can be pointed out again that a feature of the present invention is the operation of a flash EEPROM system by the memory controller as if a disk drive. This is more than making the controller look like a disk drive to the computer system, as the Burke reference says it is doing, but claims 98 and 99 define organizing and operating the flash EEPROM cell array in ways similar to that of a magnetic disk drive memory.

Claims 85-91

Reconsideration of the rejection of claims 85-91 is respectfully requested. These claims stand rejected as obvious over a combination of the Burke and Yorimoto *et al.* references. They are submitted as patentable for the same reasons stated above with respect to this combination of these same references applied to claims 79-84.

Claims 92-97

Independent claim 92 has been rejected as obvious over a combination of the cited Burke and Yorimoto *et al.* references. It is submitted that claim 92 is patentable on the ground that the Burke reference does not implicitly operate, as asserted in the

Examiner's Action, with its memory divided into sectors in the manner claimed. His 64K groups of cells are not intended to emulate disk drive sectors. It is therefore submitted that it would not have been obvious to partition any such groups into user and overhead data portions in accordance with the Yorimoto *et al.* reference, as alleged in the Examiner's Action.

Response is required to the characterizations of the Burke reference that were made in the paragraph bridging pages 8 and 9 of the Examiner's Action. No disclosure of sector addressing signals in the manner claimed is found in the Burke reference. The Burke reference does express a purpose to emulate a disk drive by appearing as a disk drive on the side of its controller that interfaces with the host computer system. But this does not make it implicit, it is submitted, that the semiconductor memory, on an opposite side of the memory controller, be divided into disk like sectors that are erasable together as a unit, contrary to what is alleged in the Examiner's Action. The type of memory disclosed in the Burke reference is made of an array of volatile dynamic RAM cells which are not erased in blocks since such cells lose their charge over time and are periodically refreshed in order to maintain their charge. The Burke system even provides for such refresh (see paragraph bridging pages 11 and 12, for example) in order to prevent their erasure.

Nor does the cited Yorimoto *et al.* reference suggest a semiconductor memory array that is divided into sectors of cells that are erased as a unit. The fact that Yorimoto *et al.* describe using an EEPROM cell array does not necessarily mean that any division of the cells into logical groups results in all cells of a group being erased together as a unit. Some EEPROM systems in the prior art operate like normal RAM systems, without the sector organization defined in claim 92.

It cannot be agreed that Official Notice is appropriately taken of alleged facts (1) through (3) of the first full paragraph of page 9. It is requested, if these rejections are continued, that appropriate prior art references be cited in support of these alleged facts, in order that a specific situation is presented to which a response can be made.

The analysis given on pages 9-11 of the Examiner's Action of the obviousness of claim 92 over the cited Burke and Yorimoto *et al.* references is submitted to be based upon erroneous factual assumptions. The fact that Burke looks to the host system as a disk drive does not make it necessary for his controller to actually operate the volatile RAM memory with the same sector characteristics as a disk drive, because that is such a different way than RAM memory is normally operated. No part of Burke's dynamic RAM cell array is erasable as a unit. To say that such a memory array is, in addition to not being described by Burke, erased in sectors is contrary to the nature of the memory cells being used. There is also no requirement that appears to exist in the Burke system to store overhead information as part of any such sector. What Burke's controller seems to do well, at least in his description, is to appear to the host system to be a disk drive memory while operating the dynamic RAM array in accordance with its particular characteristics. The fact that Burke describes emulating a disk drive does not necessarily mean, nor does it suggest, that his semiconductor array is operated with disk like attributes; namely, being divided into the claimed sectors, with overhead data (headers) stored in the individual sectors to which they pertain, usable sectors being swapped for unusable sectors, etc.

Further, the Yorimoto *et al.* reference does not suggest partitioning its EEPROM cell array into sectors that simulate those of a disk memory, as alleged in the Examiner's Action. No discussion has been noted in the Yorimoto *et al.* reference of erasing the cells within such sectors as a unit. It could be that Yorimoto *et al.* contemplated erasing the entire memory at once, which was quite common a few years ago. What is being claimed in claim 92 of the present application is a flash EEPROM cell array that is operated by its controller with characteristics that are like that of a disk drive. The suggestion of such a structure is simply not made by either of the cited Burke or Yorimoto *et al.* references.

Additionally, claim 92 has been amended to make clearer that the memory system operates to read the overhead data (header)

of an addressed sector before user data is either written to or read from the user data portion of the sector. This is another feature that departs from the usual operation of a semiconductor memory to make the flash EEPROM system operate as a disk drive memory system, and is not disclosed in either of the Burke or Yorimoto references. It is believed to be a significant departure from normal semiconductor RAM system operation to divide a memory array into sectors that individually have user data and overhead data portions, and then to read the overhead data from an addressed sector before user data is read from or written to the addressed sector. It is especially nonobvious to read a semiconductor memory sector's overhead data (header) before writing user data to that sector.

The Examiner's Action, however, in paragraphs g. and h. of page 10, paraphrase this claimed feature as prior art of which Official Notice is being taken. It is respectfully submitted that this is not a proper analysis of what one skilled in the art would have been led, prior to April 13, 1989, to find obvious. Rather, these statements merely allege obviousness without providing any factual basis to support the allegation. For example, what would have led one of ordinary skill in the art to recognize a need to validate the sector by first reading the overhead data from that sector? It is respectfully submitted that it is not enough to merely state, in a conclusionary manner and without reference to evidence of prior art, that a claimed difference over the prior art is obvious.

Claims 93-97, dependent upon claim 92, stand rejected as does claim 92 but with the Nozawa *et al.* patent additionally used to form obviousness rejections. But Nozawa *et al.* describe a disk drive memory system and do not, it is respectfully submitted, suggest ways to modify the Burke memory cell array to meet the terms of the claims. Since the Burke system does not operate his dynamic RAM cell array with disk like sector characteristics, as claimed, it is submitted that Nozawa *et al.* would not have suggested to one of ordinary skill in the art any modification of the Burke reference that could have resulted in the system defined by any of claims 93-97. Particularly, it is submitted that one

ordinarily skilled in the art would not have considered it obvious to use a disk drive sector pointing technique for substituting usable sectors for unusable sectors in the system of Burke that operates its dynamic RAM cell array without disk like sectors.

Claims 116-127

Independent claim 116 also stands rejected on the ground of obviousness over the cited Burke and Yorimoto *et al.* references. Claim 116 is similar in structure to claim 92 but is more specific in reciting flash EEPROM sector substitution. Claim 116 is also being amended to make clear that the addressed sector has its overhead data read before user data is either read from or written into that sector. Dependent claims 117, 121 and 124 stand rejected over the Burke and Yorimoto *et al.* patents, as with parent claim 116, plus the Nozawa *et al.* patent. Claim 116 and its dependent claims 117-127 are submitted to be patentable for the same reasons given above in support of the patentability of claim 92 and its dependent claims 93-97. The taking of Official Notice of certain prior art "facts" to reject claims 116-127 is submitted to be improper.

New Claims 128-143

New independent claim 128 includes use of a flash EEPROM cell array divided into separately erasable sectors that are erasable together as a unit. Overhead data is stored in each sector. A write operation is conducted by first reading overhead data from the addressed sectors and thereafter writing the user data and other overhead data. A read operation includes reading overhead data of a sector before reading its user data. These elements of novelty, most of which are extensively discussed above with respect to other claims, are submitted to render claim 128 patentable. New claims 129-143 add other novel elements, most of which have also been discussed above with respect to the prior art.

Conclusion

For the reasons stated above, it is submitted that the present application is in condition for allowance. However, should

the Examiner have any further matters that need to be resolved, the undersigned attorney would appreciate a telephone call.

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Respectfully submitted,

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